Lecture 4: Verification of Weak Memory Models

Part 2: Robustness against TSO

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Dekker's Protocol

Synchronise access of two threads to their critical sections

Dekker's mutual exclusion protocol

$t_1 : q_0 \longrightarrow q_1 \longrightarrow cs \quad t_2 : \mathbf{q_0} \longrightarrow \mathbf{q_1} \to \mathbf{q_2} \longrightarrow \mathbf{cs}$

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- **Indicate wish to enter** Write own variable x to 1

$$t_1 : q_0 \xrightarrow{(w,x,1)} q_1 \longrightarrow cs \qquad t_2 : \mathbf{q_0} \longrightarrow \mathbf{q_1} \rightarrow \mathbf{q_2} \longrightarrow \mathbf{cs}$$

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- **Symmetry** Second thread behaves similarly

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- What is the semantics of this program?

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- What is the semantics of this program?
- Depends on the hardware architecture!

Sequential Consistency Semantics

Sequential Consistency memory model [Lamport 1979]

- Threads directly write to and read from memory
- Programmers often rely on this intuitive behaviour

Sequential Consistency Semantics

Sequential Consistency memory model [Lamport 1979]

- Take view from memory

Sequential Consistency semantics of Dekker's protocol

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Next: t_1 writes x to 1

$t_1 : q_0$

$t_2 : \mathbf{q_0}$

M
$x = 0$
$y = 0$

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$$(w, x, 1)$$

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Next: t_1 reads 0 from y

$t_1 : q_1$

$t_2 : \mathbf{q_0}$

$$\boxed{\begin{array}{c} M \\ x = 1 \\ y = 0 \end{array}}$$

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$$(w, x, 1).(r, y, 0)$$

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Next: t_2 writes y to 1

$t_1 : cs$

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Next: t_2 executes fence **f**

$$t_1 : cs \qquad t_2 : \mathbf{q_1} \qquad \boxed{\begin{array}{c} M \\ x = 1 \\ y = 1 \end{array}}$$

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Next: t_2 cannot read 0 from x

$t_1 : cs$

$t_2 : \mathbf{q_2}$

$$\boxed{\begin{array}{c} M \\ x = 1 \\ y = 1 \end{array}}$$

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$t_1 : cs$

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Mutual exclusion holds!

Total Store Ordering Semantics

- Buffers reduce latency of memory accesses

Total Store Ordering semantics of Dekker's protocol

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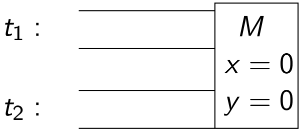

Total Store Ordering Semantics

- Buffers reduce latency of memory accesses
- Total Store Ordering architectures have write buffers

Total Store Ordering semantics of Dekker's protocol

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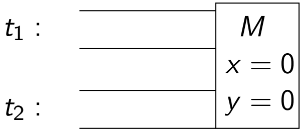

Total Store Ordering Semantics

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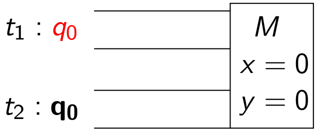
Next: t_1 writes $(w, x, 1)$ to its buffer



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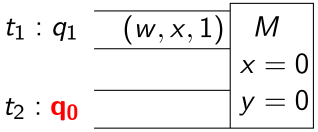
Next: t_2 writes $(\mathbf{w}, \mathbf{y}, \mathbf{1})$ to its buffer



Total Store Ordering Semantics

- Reads prefetch last value written to x from buffer

Total Store Ordering semantics of Dekker's protocol

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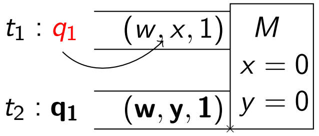
Next: t_1 fails to read $(r, y, 0)$ from its buffer



Total Store Ordering Semantics

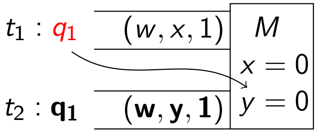
- Reads prefetch last value written to x from buffer, if exists

$(r, y, 0)$

Total Store Ordering semantics of Dekker's protocol

$t_1 : q_0 \xrightarrow{(w,x,1)} q_1 \xrightarrow{(r,y,0)} cs \qquad t_2 : \mathbf{q}_0 \xrightarrow{(\mathbf{w},\mathbf{y},\mathbf{1})} \mathbf{q}_1 \xrightarrow{\mathbf{f}} \mathbf{q}_2 \xrightarrow{(\mathbf{r},\mathbf{x},\mathbf{0})} \mathbf{cs}$

Next: t_1 reads $(r, y, 0)$ from memory



Total Store Ordering Semantics

- Reads prefetch last value written to x from buffer, if exists
- Fences forbid prefetches

$(r, y, 0)$

Total Store Ordering semantics of Dekker's protocol

$t_1 : q_0 \xrightarrow{(w,x,1)} q_1 \xrightarrow{(r,y,0)} cs \qquad t_2 : \mathbf{q}_0 \xrightarrow{(\mathbf{w},\mathbf{y},\mathbf{1})} \mathbf{q}_1 \xrightarrow{\mathbf{f}} \mathbf{q}_2 \xrightarrow{(\mathbf{r},\mathbf{x},\mathbf{0})} \mathbf{cs}$

Next: t_2 cannot execute fence **f** while buffer not empty

$t_1 : cs$	$(w, x, 1)$	M
		$x = 0$
$t_2 : \mathbf{q_1}$	$(\mathbf{w}, \mathbf{y}, \mathbf{1})$	$y = 0$

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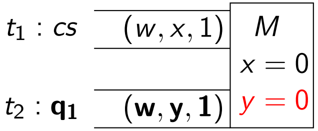
Next: memory updates $(\mathbf{w}, \mathbf{y}, \mathbf{1})$ from buffer of t_2



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$$\color{red}{(r, y, 0)}\color{black}\,.(\mathbf{w}, \mathbf{y}, \mathbf{1})$$

Total Store Ordering semantics of Dekker's protocol

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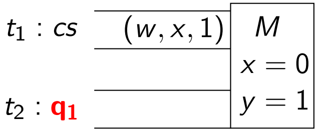

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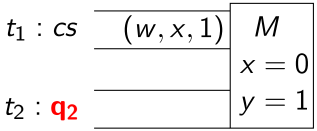

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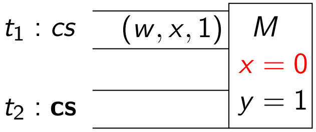

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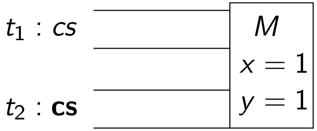

Total Store Ordering Semantics

- Memory sees actions out of program order

$$\begin{tikzcd}[column sep=small] {\color{red}(r,y,0)} \arrow[r, phantom, "."] & (\mathbf{w},\mathbf{y},\mathbf{1}).\mathbf{f}.(\mathbf{r},\mathbf{x},\mathbf{0}) \arrow[r, phantom, "."] & {\color{red}(w,x,1)} \arrow[ll, bend right, start anchor=north east, end anchor=north east] \end{tikzcd}$$

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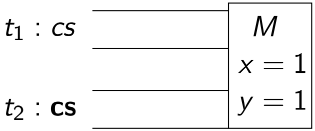

Mutual exclusion fails!

Robustness against TSO

[Burckhardt, Musuvathi, 2008], [Owens, 2010], [Alglave, Maranget, 2011]

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  Preservation of the traces [Shasha, Snir, 88]

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- Reducible to state reachability: decidable but highly complex!
- Trace-Robustness:
  Preservation of the traces [Shasha, Snir, 88]
- Checking trace-robustness is less costly than checking state-robustness!

Traces

Given a computation τ, consider:

- Program order $\rightarrow_{\mathtt{po}}$: Order of actions issued by one thread.
- Store order $\rightarrow_{\mathtt{st}}$: Order of writes to a same variable (by different threads).
- Source relation $\rightarrow_{\mathtt{src}}$: *write* is source of *load*.
- The trace $T(\tau)$ is defined by the union of $\rightarrow_{\mathtt{po}}$, $\rightarrow_{\mathtt{st}}$, $\rightarrow_{\mathtt{src}}$.

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- Given a memory model M, and program P, $Tr_M(P)$ is the set of all traces associated with computations of P under M.
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- Happen-Before relation $\rightarrow_{\texttt{hb}}$: union of all relations above.
- **Thm** [SS88]:

  $T(\tau) \in Tr_{SC}(P)$ *if and only if* $\rightarrow_{\texttt{hb}}$ *is acyclic.*

Example

Dekker's protocol

$$\begin{tikzcd}
T(\tau) & (w, x, 1) \arrow[d] & (\mathbf{w}, \mathbf{y}, \mathbf{1}) \arrow[d] \\
 & (r, y, 0) \arrow[ur] & \mathbf{f} \arrow[d] \\
 & & (\mathbf{r}, \mathbf{x}, \mathbf{0}) \arrow[uul]
\end{tikzcd}$$

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 & (r,y,0) \arrow[rru] & & \mathbf{f} \arrow[d] \\
 & & & (\mathbf{r},\mathbf{x},\mathbf{0}) \arrow[lluu]
\end{tikzcd}$$

Dekker's protocol is not robust, τ is a violation

Deciding Robustness

Shasha and Snir do not give an algorithm to find cyclic traces !

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- Reduce to SC reachability in instrumented programs
- Source-to-source translation with linear overhead
- Quadratic number of reachability queries
- Works for unbounded buffers and arbitrarily many threads
- P/EXP-SPACE-complete

Roadmap

- Locality of robustness — only one thread uses buffers
- Robustness iff no attacks
- Find attacks with SC(!) reachability

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Minimal Violations

Goal

Show that we can restrict ourselves to

violations where only one thread reorders its actions

Minimal Violations

TSO computations from rewriting

Reorder $(w,x,1).(r,y,0) \curvearrowright_{re} (r,y,0).(w,x,1)$

Prefetch $(w,x,v).(r,x,v) \curvearrowright_{pf} (w,x,v)$

Minimal Violations

TSO computations from rewriting

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Intuition: violations as close to SC as possible

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Minimal violations have good properties!

Helpful Lemma for Minimal Violations

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Consider minimal violation $\alpha.b.\beta.a.\gamma$ *where* b *has overtaken* a

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$$b_i \rightarrow_{src/st/cf} b_{i+1} \qquad \text{or} \qquad b_i \rightarrow_p^+ b_{i+1}$$

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Example (Computation in Dekker's protocol is minimal)

$$\underbrace{(r, y, 0).(\mathbf{w}, \mathbf{y}, \mathbf{1}).\mathbf{f}.(\mathbf{r}, \mathbf{x}, \mathbf{0}).(w, x, 1)}_{\rightarrow_{hb}}$$

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Theorem (Locality of Robustness)

In a minimal violation, only a single thread uses rewriting

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Case 1: no interference

$$\begin{tikzcd}
{} \arrow[r, dash] & r_j \arrow[r, dash] & w_j \arrow[l, bend right] \arrow[r, dash] & r_i \arrow[r, dash] & w_i \arrow[l, bend right] \arrow[r, dash] & {}
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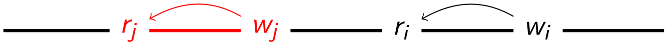

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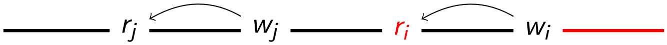

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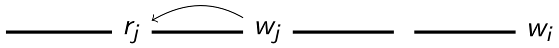

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Read r_i not involved, delete everything from r_i on
Saves a reordering, contradiction to minimality

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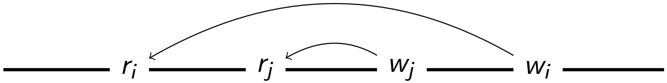

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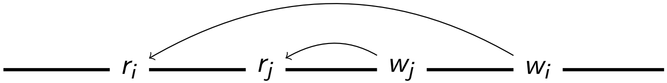

Argumentation similar, delete again r_i

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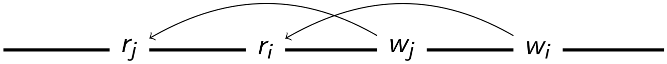

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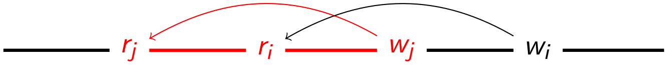

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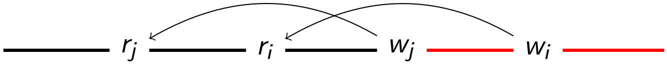

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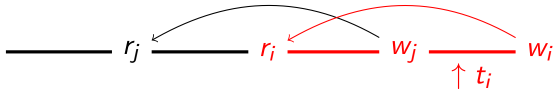

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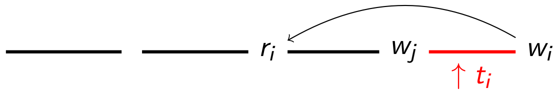

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Read r_j not on this cycle, delete it, contradiction

Roadmap

- Locality of robustness — only one thread uses buffers
- Robustness iff no attacks
- Find attacks with SC(!) reachability

Characterization of Robustness via Attacks

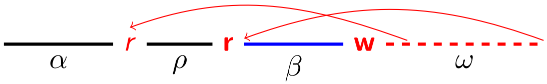
Goal

Reformulate Robustness in terms of a simpler problem:

absence of feasible attacks

Characterization of Robustness via Attacks

Observation
If Prog not robust, there are these violation:



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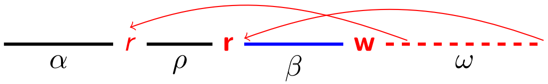

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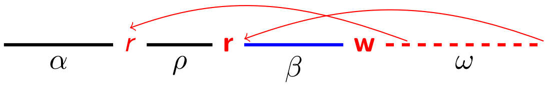

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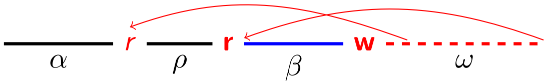

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Intuition

Two data races $\mathbf{r}$, *first*(β) and *last*$(\beta), \mathbf{w}$

Characterization of Robustness via Attacks

Idea

- Fix thread, write instruction, read instruction
- Given these parameters, find a violation as above

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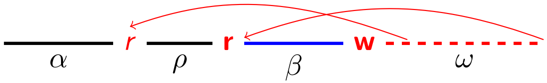
An attack is a triple $A = (\mathit{thread}, \mathit{write}, \mathit{read})$.
A TSO witness for attack A is a computation as above:



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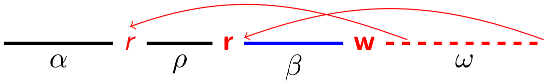

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Program Prog is robust if and only if no attack has a TSO witness.

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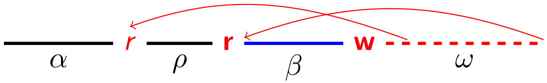

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The number of attacks is quadratic in the size of Prog.

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Finding TSO witnesses with SC reachability

Fix an attack $A = (\mathit{thread}, \mathit{write}, \mathit{read})$

Goal

TSO witnesses for A considerably restrict reorderings,

enough to find TSO witnesses with SC reachability

Finding TSO witnesses with SC reachability

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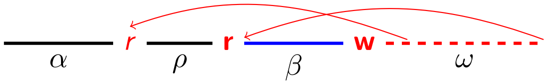
Turn TSO witness into an SC computation:



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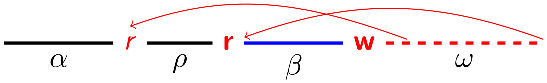
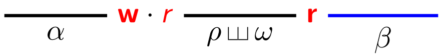


Let attacker execute under SC



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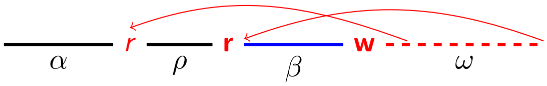

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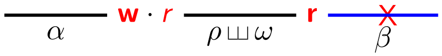

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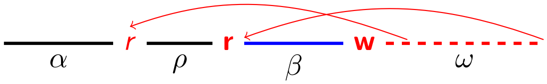

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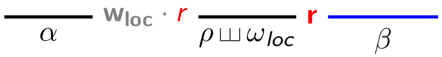
Problem Writes may conflict with helper reads

Solution Hide them from other threads


α
$\mathbf{w}_{\mathbf{loc}} \cdot r$
$\rho \sqcup \omega_{loc}$
$\mathbf{r}$
β

Finding TSO witnesses with SC reachability

Instrumentation

$$\underset{\alpha}{\underline{\qquad\qquad}}\ \mathbf{w_{loc}} \cdot r\ \underset{\rho \sqcup \omega_{loc}}{\underline{\qquad\qquad}}\ \mathbf{r}\ \underset{\beta}{\underline{\qquad\qquad}}$$

SC computation $\in$ Prog$_A$ that is instrumented for attack A

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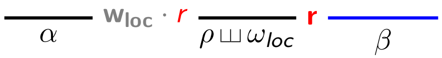

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Theorem (Soundness and Completeness)

Attack A has a TSO witness iff Prog_A reaches goal state under SC.

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- Check existence of feasible attacks.
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- Experiments: Mutex protocols, lock-free stack, work stealing queue, non-blocking write protocol, etc. Reachability queries are solved in few seconds.

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- Can be extended to NSW. What about Power, ARM?

The Programming Model: Assembler

$$
\begin{array}{lcl}
\langle \mathit{prog} \rangle & ::= & \text{prog } \langle \text{pid} \rangle \ \langle \text{thread} \rangle^* \\
\langle \mathit{thrd} \rangle & ::= & \text{thread } \langle \text{tid} \rangle \text{ regs } \langle \text{reg} \rangle^* \text{ init } \langle \text{label} \rangle \text{ begin } \langle \text{linst} \rangle^* \text{ end} \\
\langle \mathit{linst} \rangle & ::= & \langle \text{label} \rangle\text{: } \langle \text{inst} \rangle\text{; goto } \langle \text{label} \rangle \\
\langle \mathit{inst} \rangle & ::= & \langle \text{reg} \rangle \leftarrow \text{mem}[\langle \text{expr} \rangle] \mid \text{mem}[\langle \text{expr} \rangle] \leftarrow \langle \text{expr} \rangle \mid \text{mfence} \\
 & & \mid \langle \text{reg} \rangle \leftarrow \langle \text{expr} \rangle \mid \text{if } \langle \text{expr} \rangle \\
\langle \mathit{expr} \rangle & ::= & \langle \text{fun} \rangle(\langle \text{reg} \rangle^*)
\end{array}
$$

Experiments

Spin as backend model checker

Prog.	T	L	I	PA	IA1	IA2	FA	F	Spin
PetNR	2	14	18	23	2	12	9	2	0.7
PetR	2	16	20	12	12	0	0	0	0.0
DekNR	2	24	30	119	15	33	71	4	3.5
DekR	2	32	38	30	30	0	0	0	0.0
LamNR	3	33	36	36	9	15	12	6	1.1
LamR	3	39	42	27	27	0	0	0	0.0
LFSR	4	46	50	14	14	0	0	0	0.0
CLHLock	7	62	58	54	48	6	0	0	0.4
MCSLock	4	52	50	30	26	4	0	0	0.2
NBW5	3	25	22	9	7	2	0	0	0.1
ParNR	2	9	8	2	0	1	1	1	0.1
ParR	2	10	9	2	2	0	0	0	0.0
WSQ	5	86	78	147	137	10	0	0	0.7