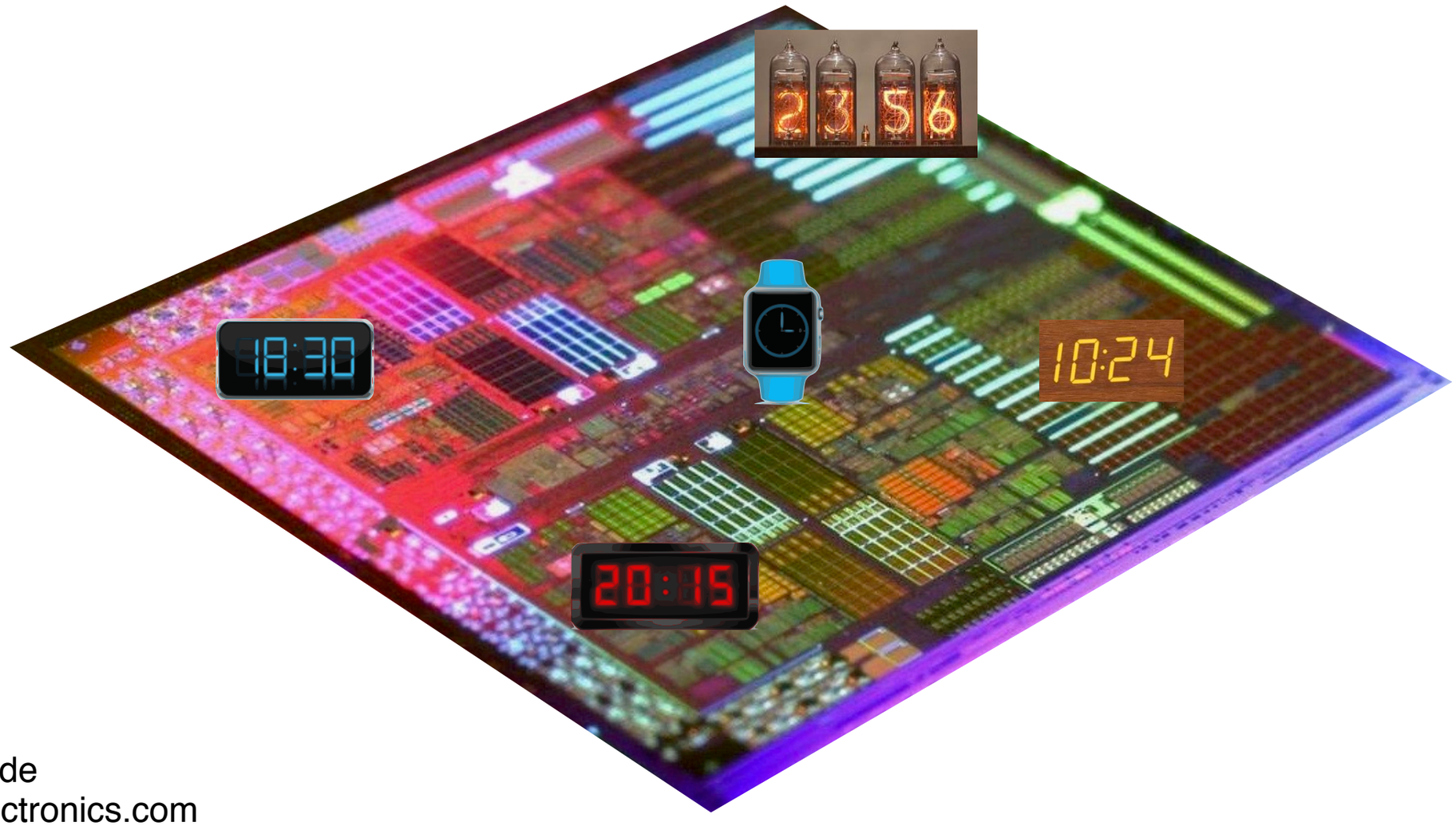
Phase Locked Loops, PLLs, for Clocking Chips



Ian W. Jones
and
Felipe A. Kuentzer

ianjones@mpi-inf.mpg.de
kuentzer@ihp-microelectronics.com
December 2020

Outline

Part 1:

- Overview
- Intro to PLLs
- Clocking with PLLs
- Analog PLLs

Part 2:

- Recap
- Digital PLLs
- Future challenges
- Summary

Recap

- Clocked chips => ease design (uniformity)
- PLLs => low jitter, stable
  => programmable
  => ratioed phase-related clocks
  => enable many forms of
  data communication
- Analog PLLs => excellent, but:
  large & high power

Outline

Part 1:

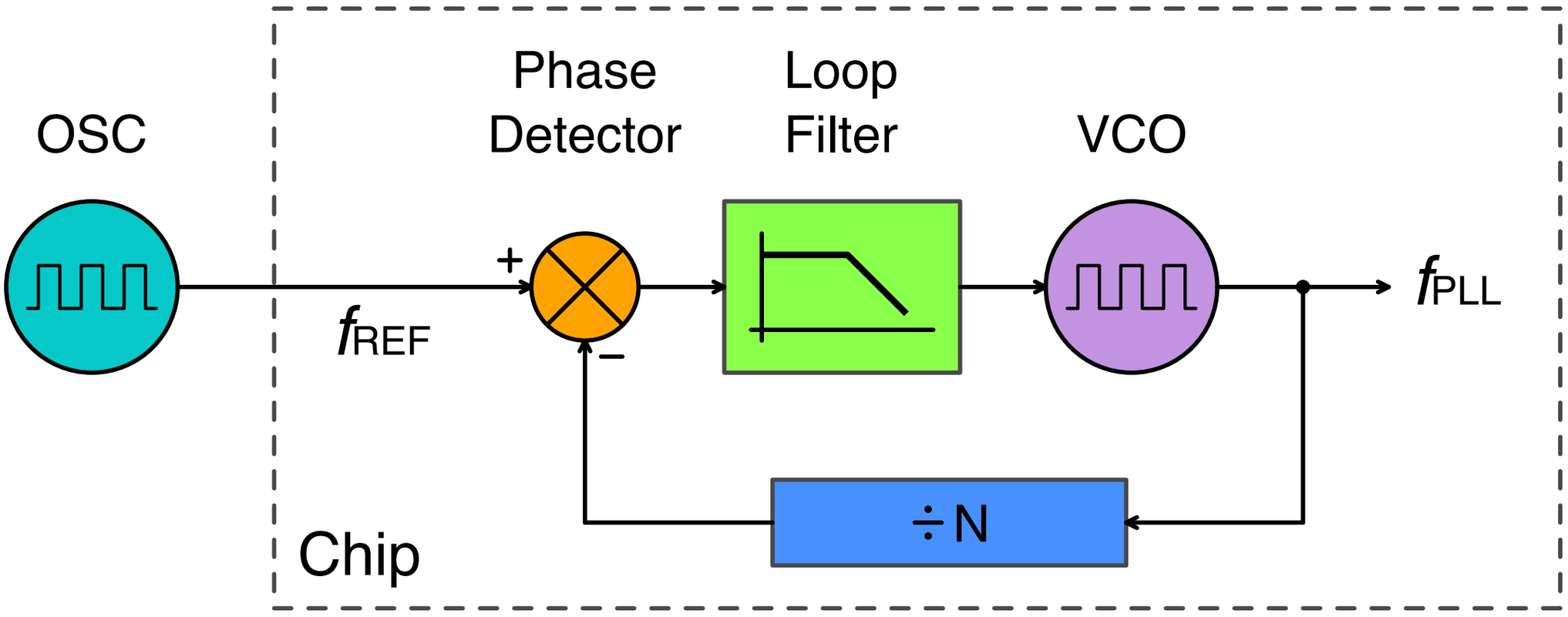
- Overview
- Intro to PLLs
- Clocking with PLLs
- Analog PLLs

Part 2:

- Recap
- Digital PLLs
- Future challenges
- Summary

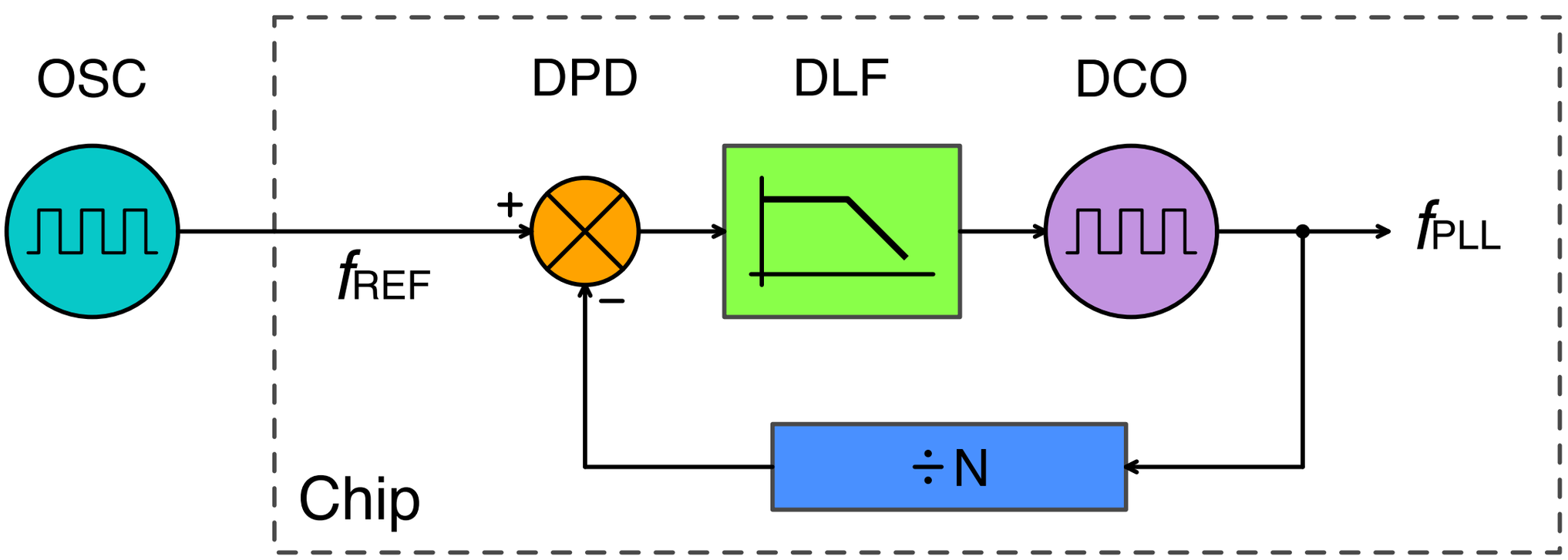
Analog PLL

$$f_{PLL} = N \times f_{REF}$$

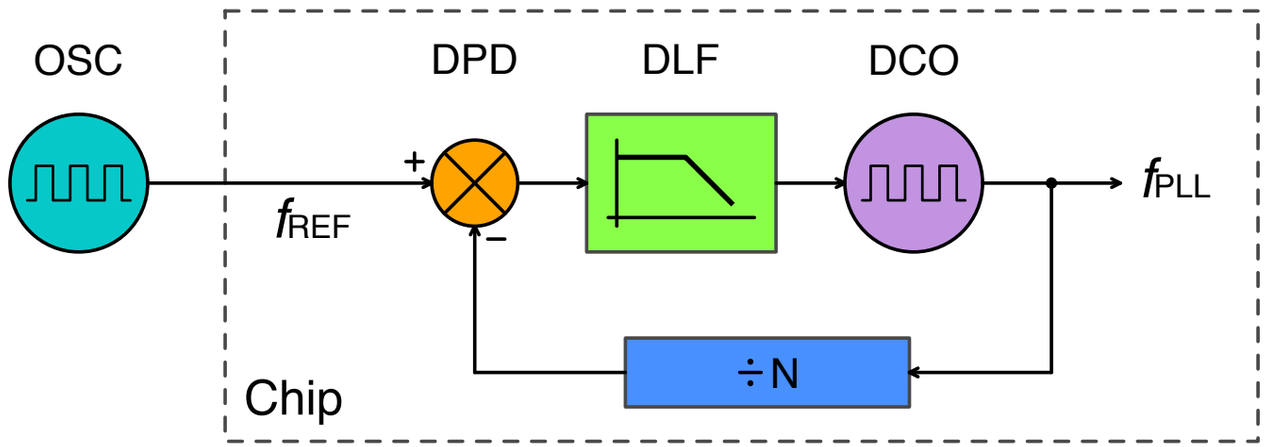


Digital PLL

$$f_{PLL} = N \times f_{REF}$$



Digital PLL Components



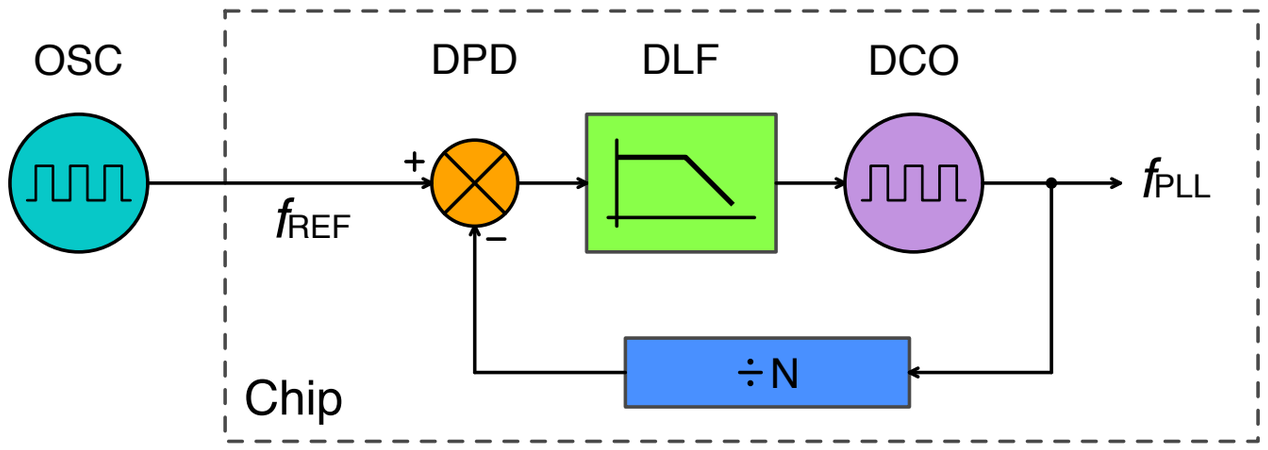
OSC – External clock reference

DCO – On-chip Digital Controlled Oscillator

DPD – Digital Phase Detector

DLF – Digital Loop Filter

Digital PLL Components



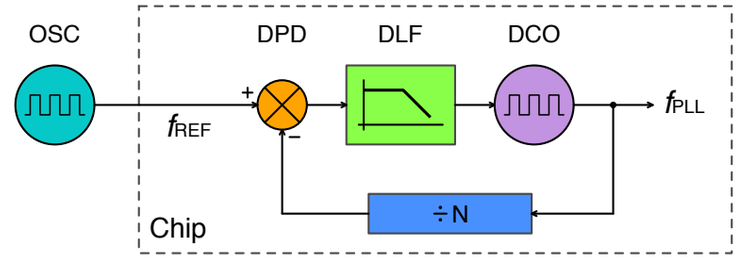
OSC – External clock reference

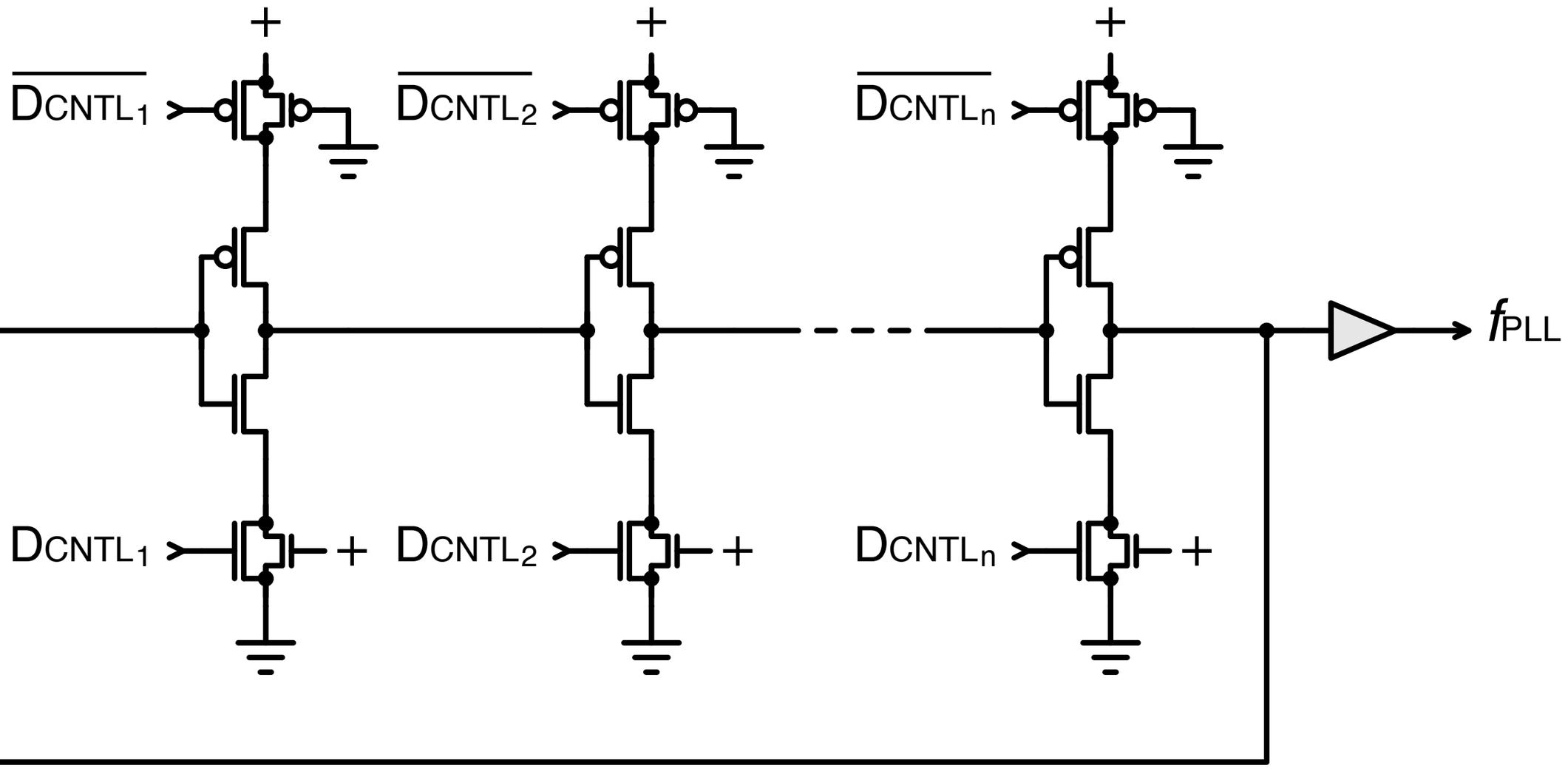
DCO – On-chip Digital Controlled Oscillator

DPD – Digital Phase Detector

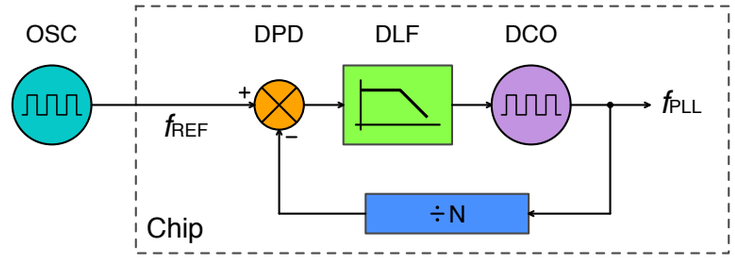
DLF – Digital Loop Filter

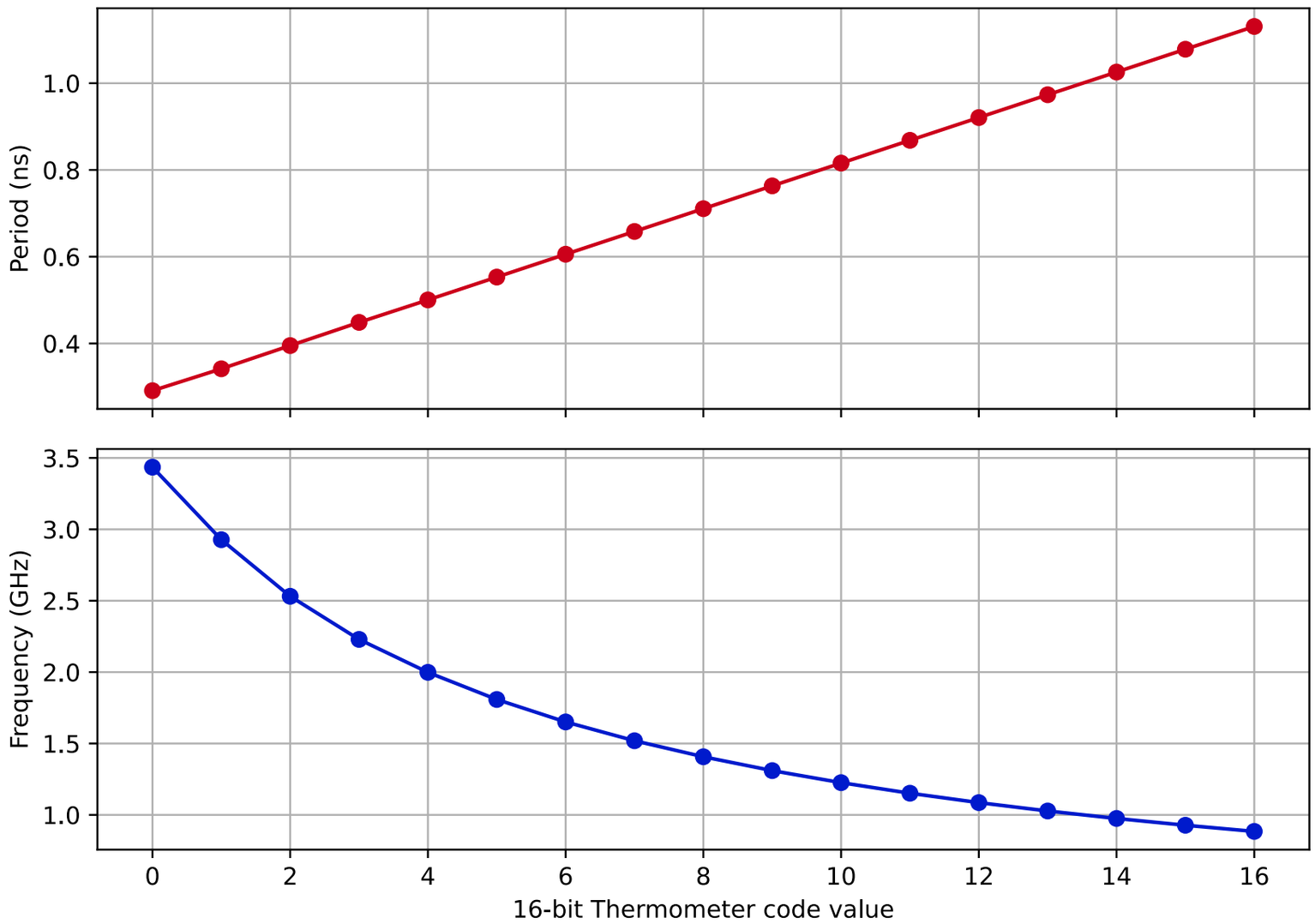
Digital Controlled Oscillator, DCO



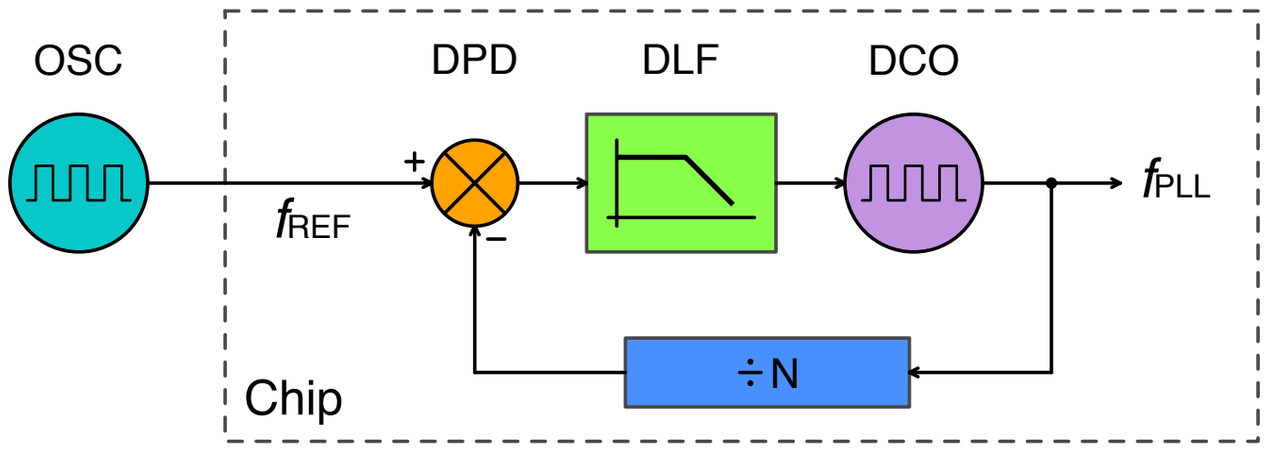


Digital Controlled Oscillator, DCO





Digital PLL Components



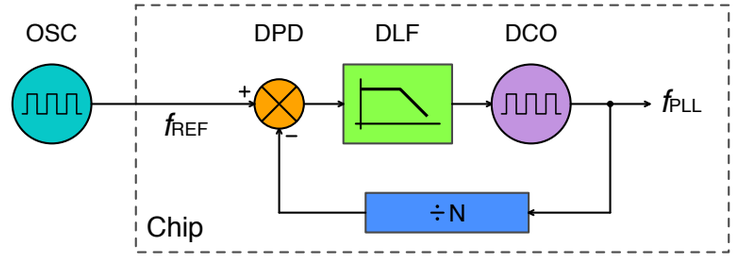
OSC – External clock reference

DCO – On-chip Digital Controlled Oscillator

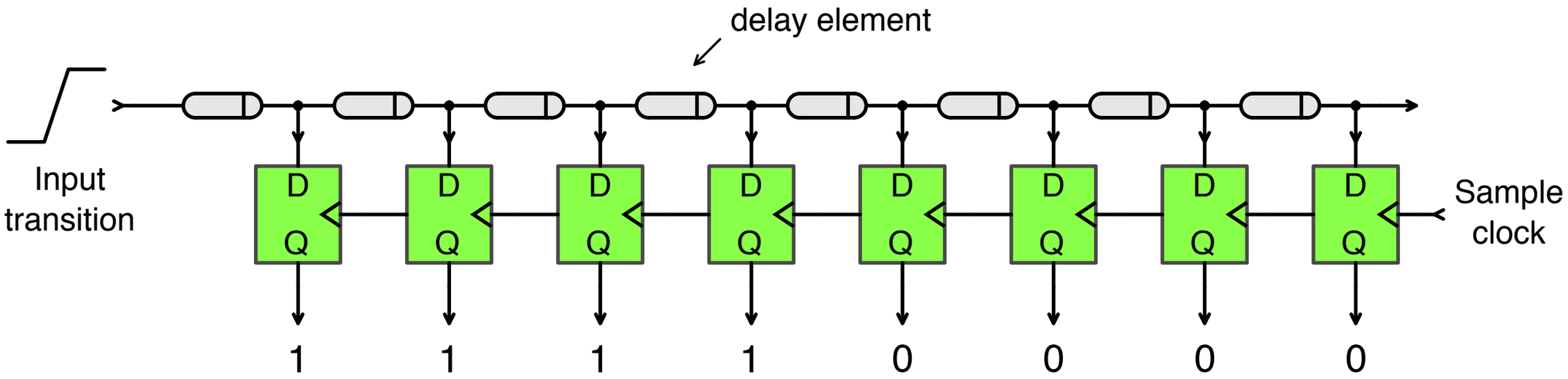
DPD – Digital Phase Detector

DLF – Digital Loop Filter

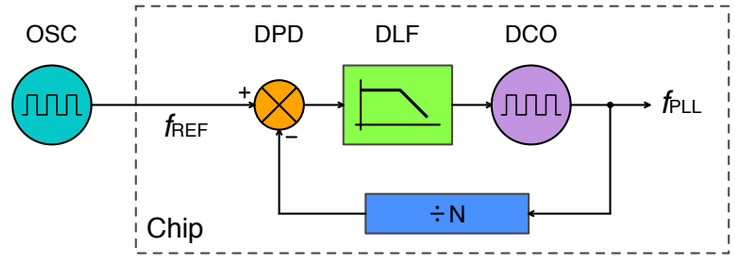
Digital Phase Detector, DPD



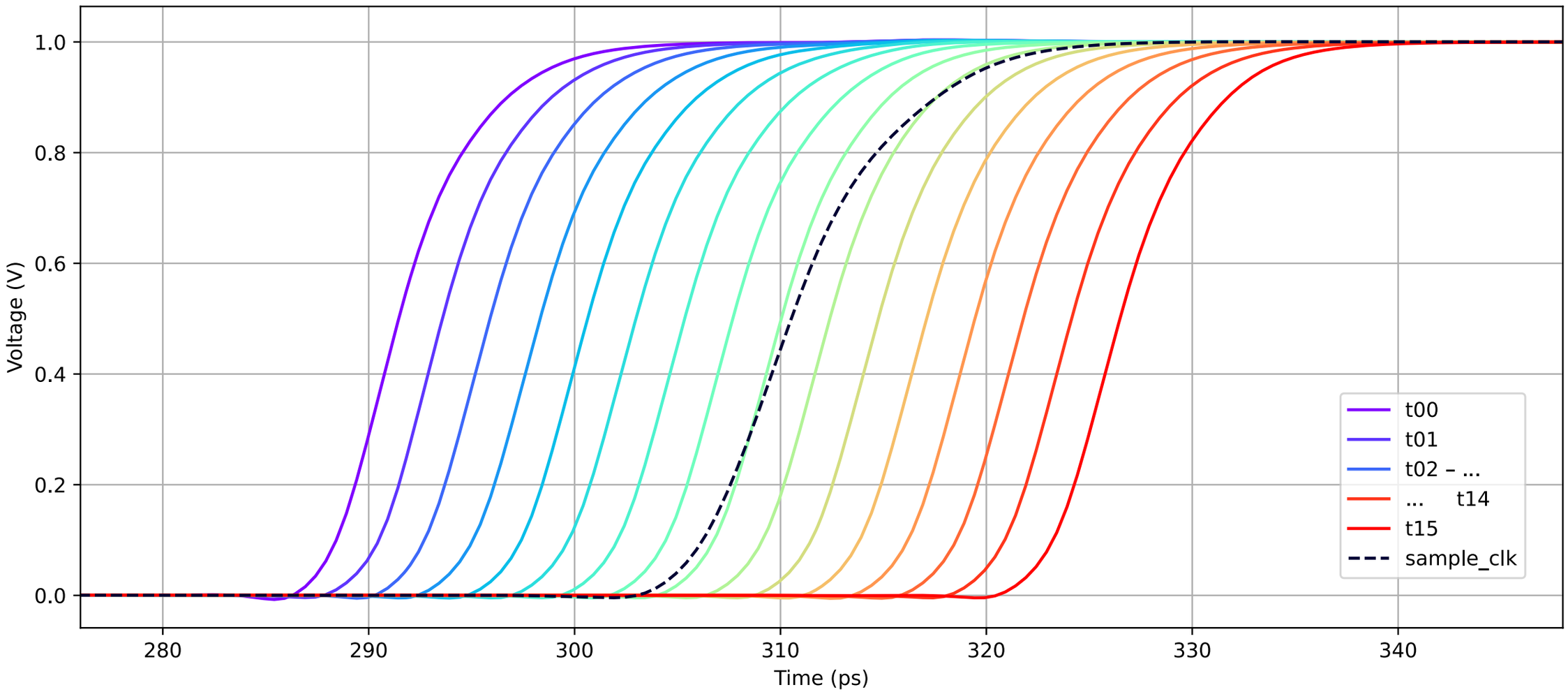
Time-To-Digital Converter, TDC:



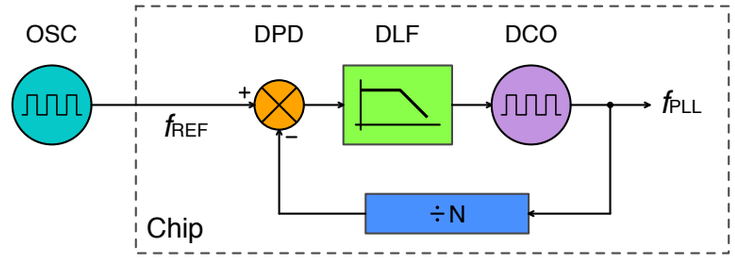
Digital Phase Detector, DPD



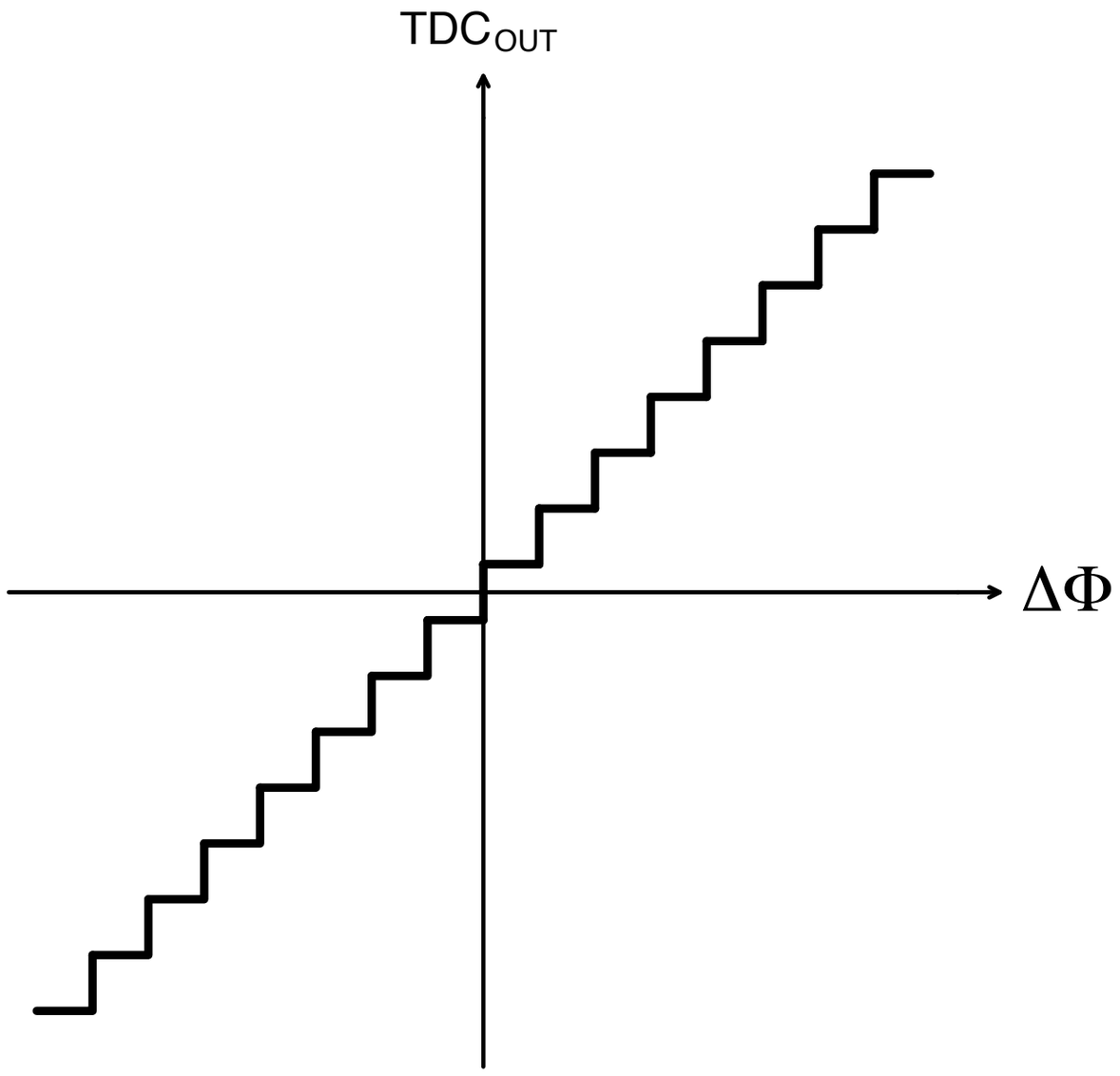
TDC waveforms:



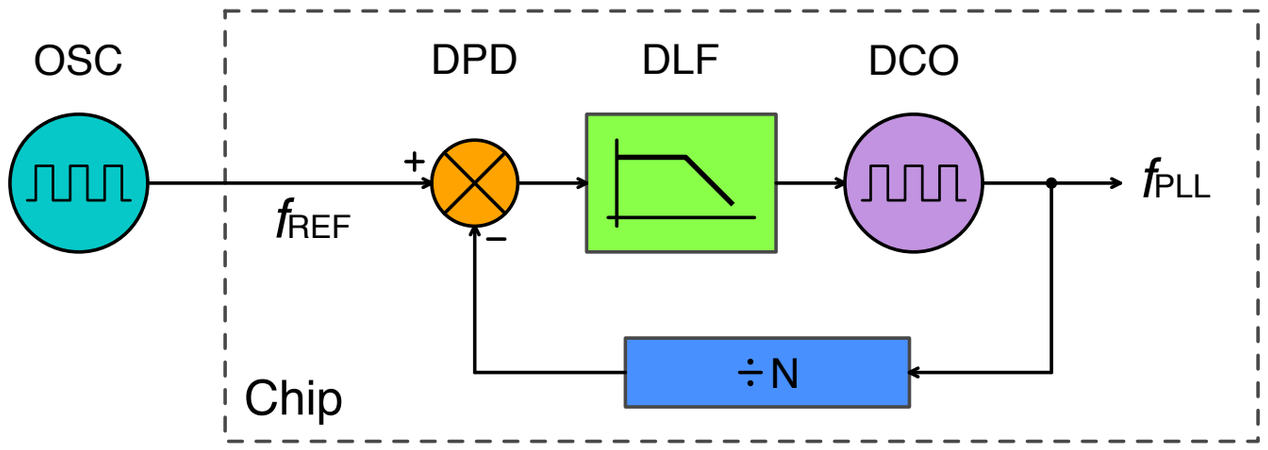
Digital Phase Detector, DPD



TDC steps:



Digital PLL Components



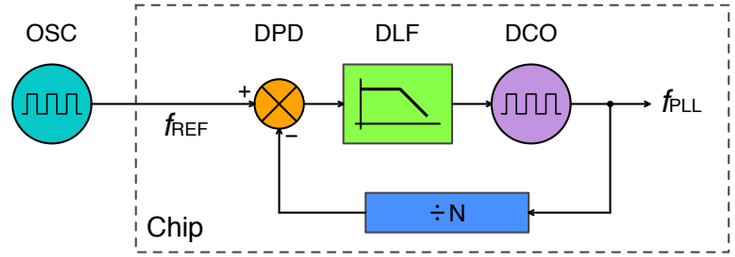
OSC – External clock reference

DCO – On-chip Digital Controlled Oscillator

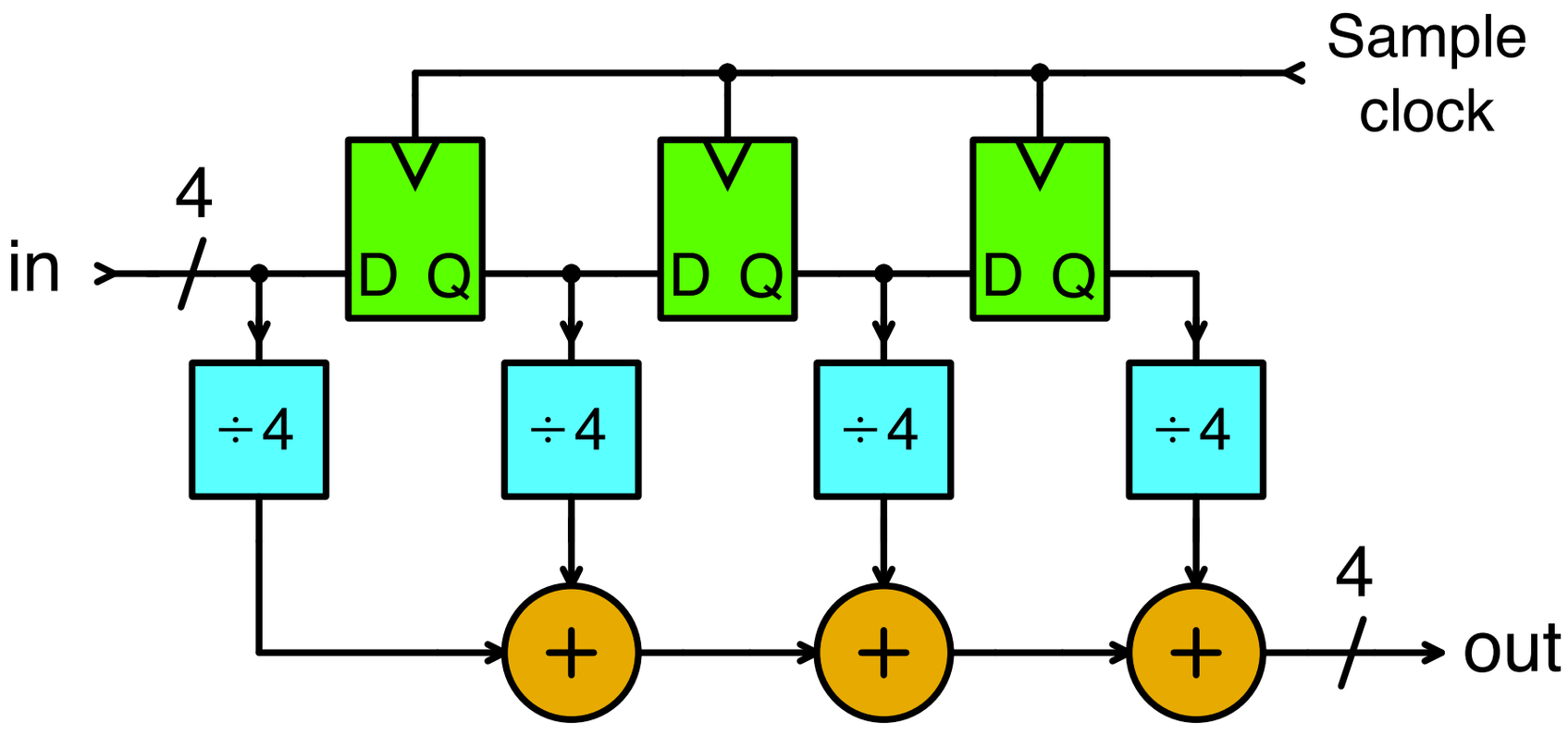
DPD – Digital Phase Detector

DLF – Digital Loop Filter

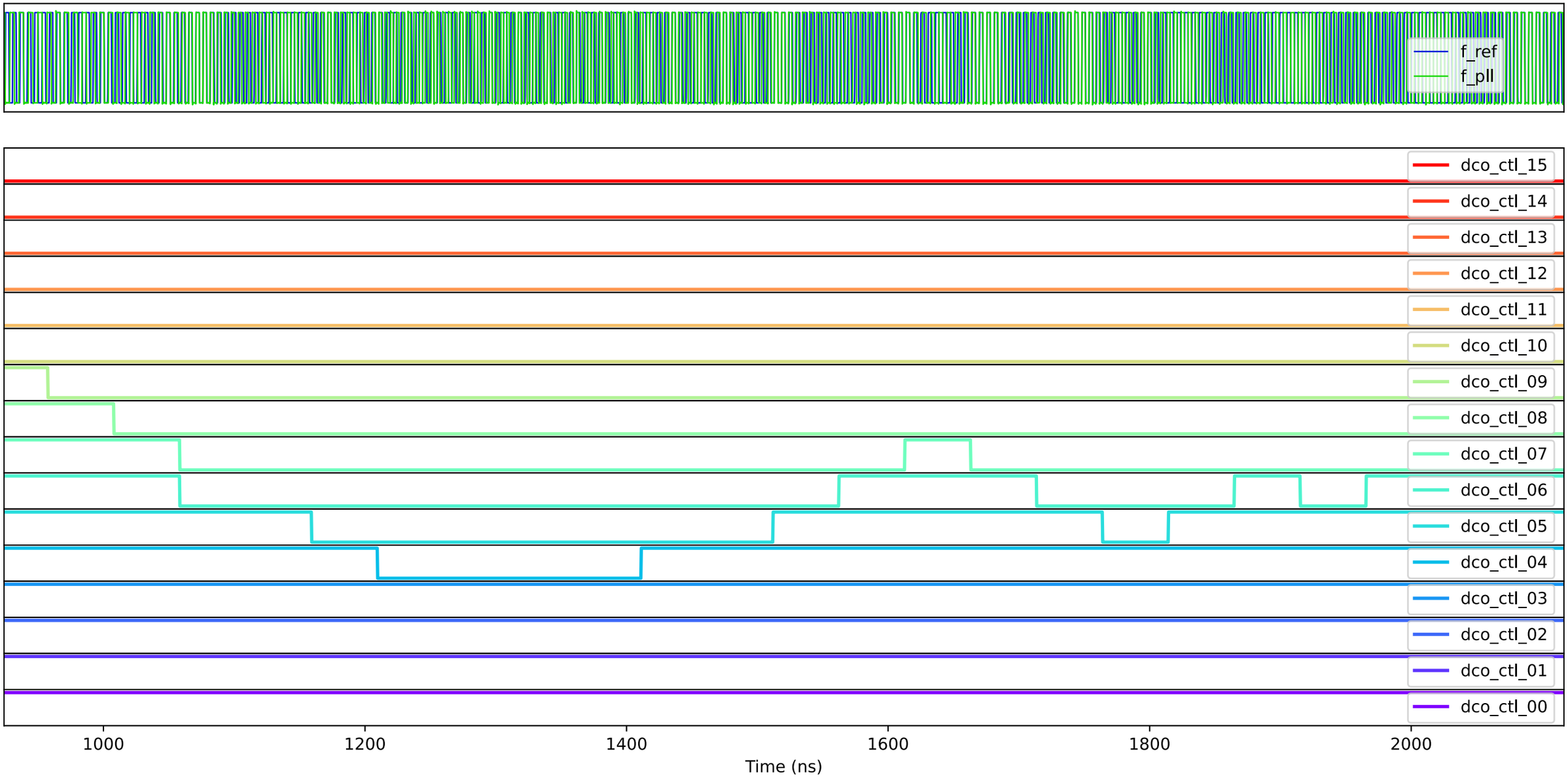
Digital Loop Filter, DLF



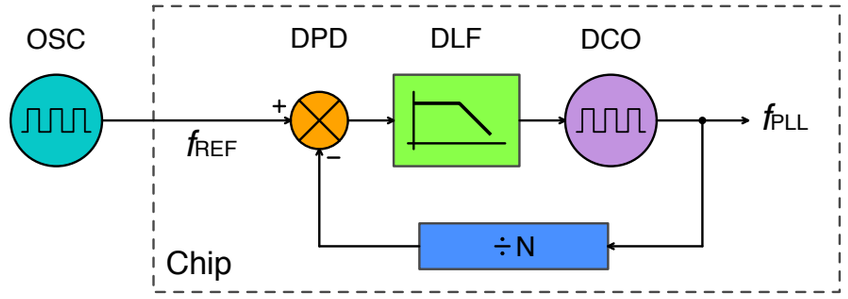
4-stage FIR low-pass filter:



Digital PLL


f_ref
f_pll
dco_ctl_15
dco_ctl_14
dco_ctl_13
dco_ctl_12
dco_ctl_11
dco_ctl_10
dco_ctl_09
dco_ctl_08
dco_ctl_07
dco_ctl_06
dco_ctl_05
dco_ctl_04
dco_ctl_03
dco_ctl_02
dco_ctl_01
dco_ctl_00
1000
1200
1400
1600
1800
2000
Time (ns)

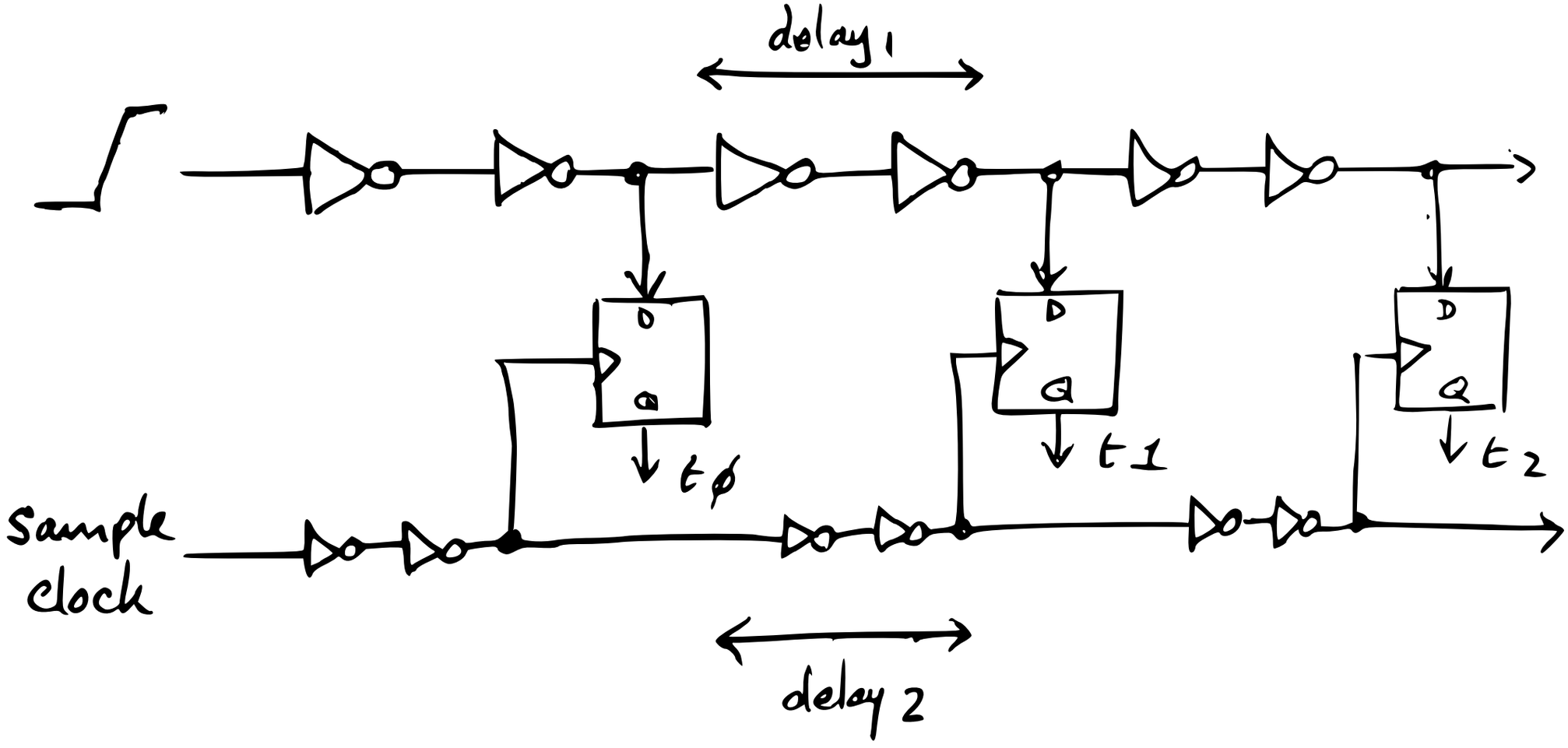
Discussion Session #1



- What needs further explanation?
- How can we improve the DPD resolution?
- What makes the digital loop filter smaller than it's analog counterpart?

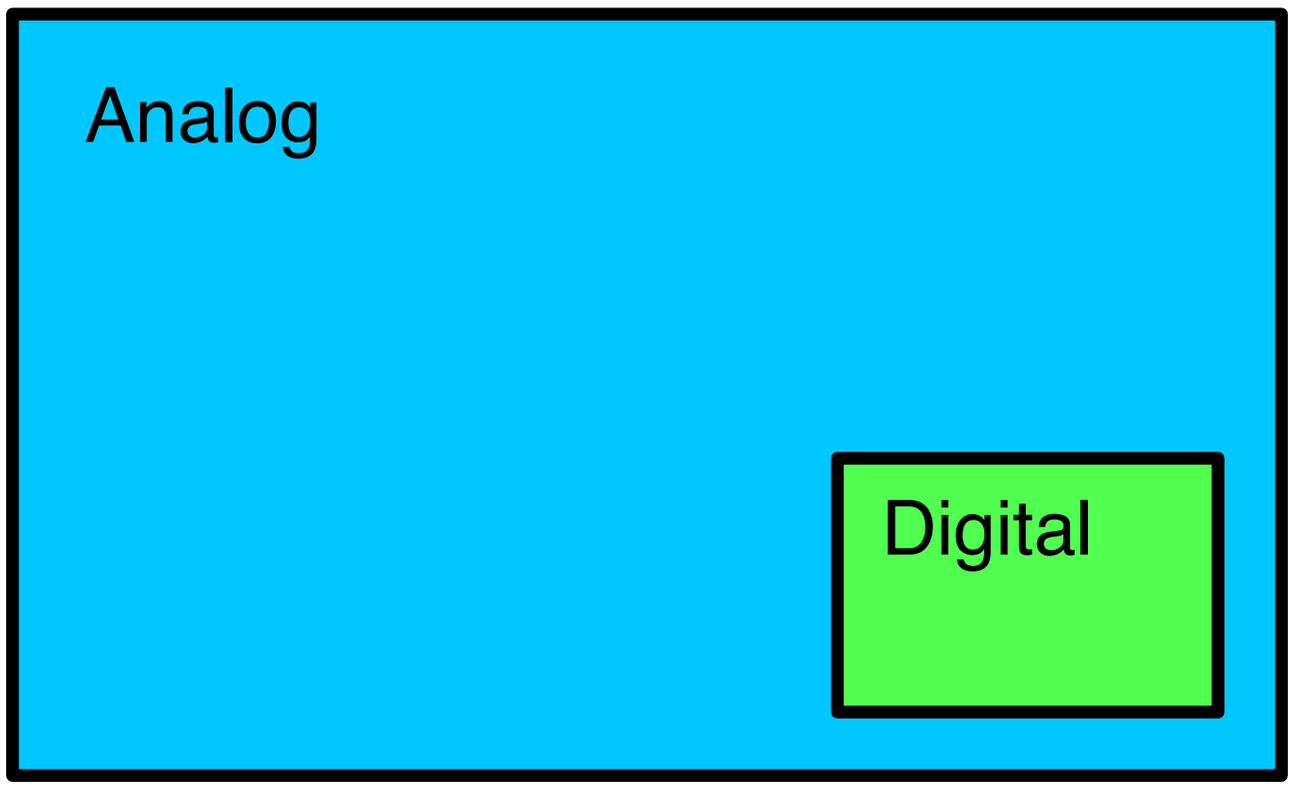
Note: Digital filter design is a whole subject in itself!

Discussion Session #1:
Vernier Tapped Delay Line



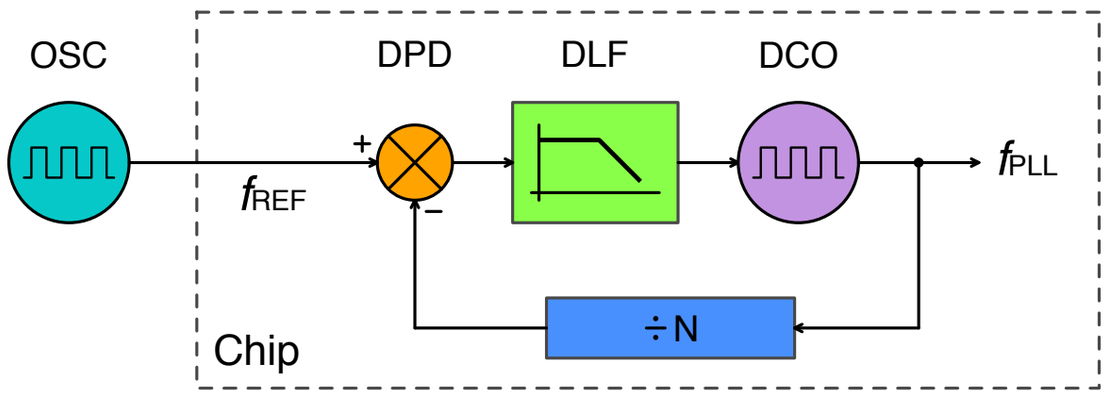
Do you see any possible problems?

Discussion Session #1:
Digital loop filter size



Digital filter can be 10x smaller than analog filter:
large capacitances required by analog filter.

Discussion Session #1



END

Return to lecture

Outline

Part 1:

- Overview
- Intro to PLLs
- Clocking with PLLs
- Analog PLLs

Part 2:

- Recap
- Digital PLLs
- Future challenges
- Summary

Clocking Challenges

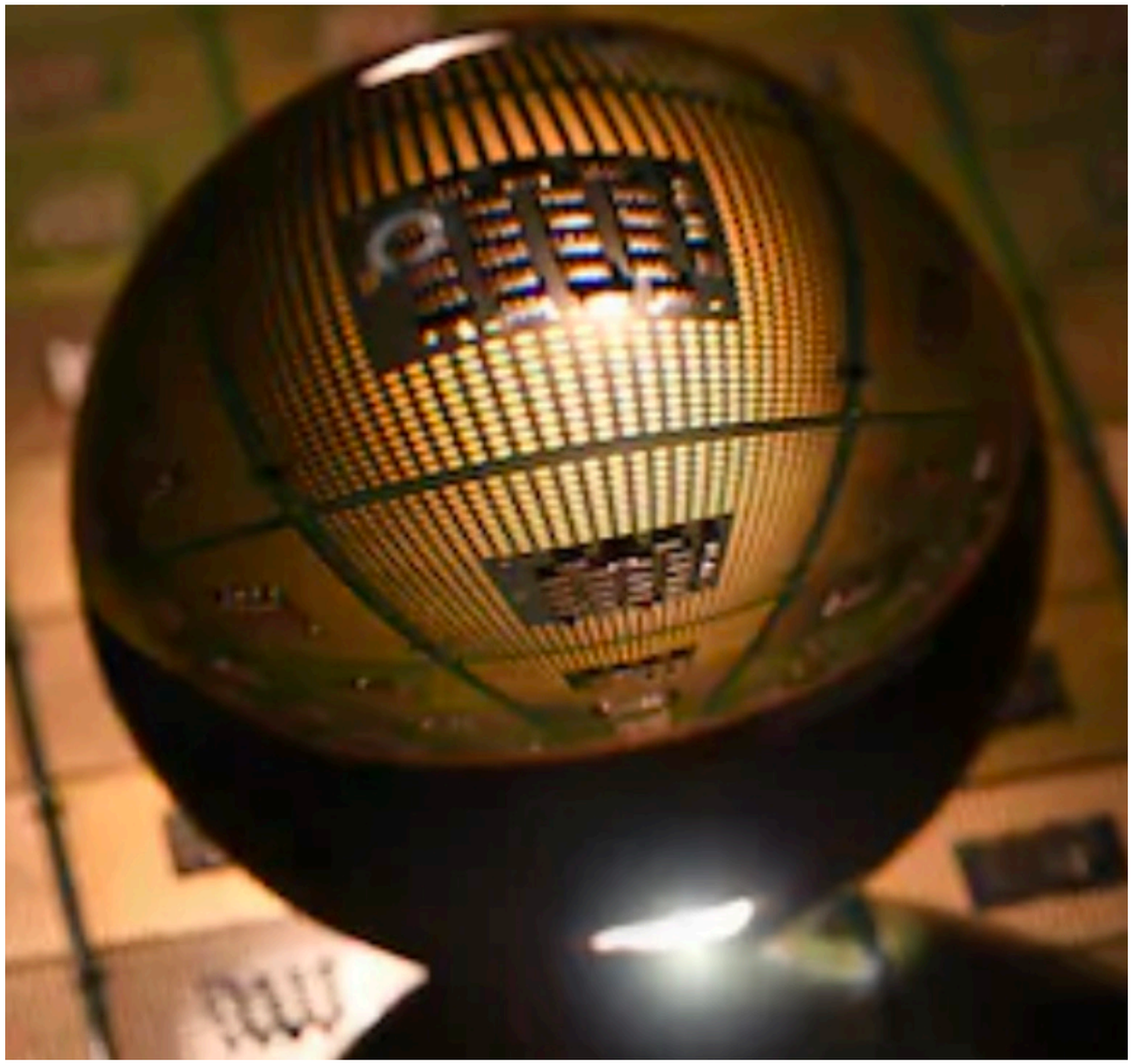
- Gate delays becoming more sensitive to supply voltage variations

  – need to quickly adjust the clock to compensate

- Cost of synchronization delays at clock domain crossings is too high

  — takes multiple clock cycles

Future



Future Chips

Technology advances bring:

– complete systems on chip

– more computing

– more clock domains

– more delay variation

Beyond PLLs

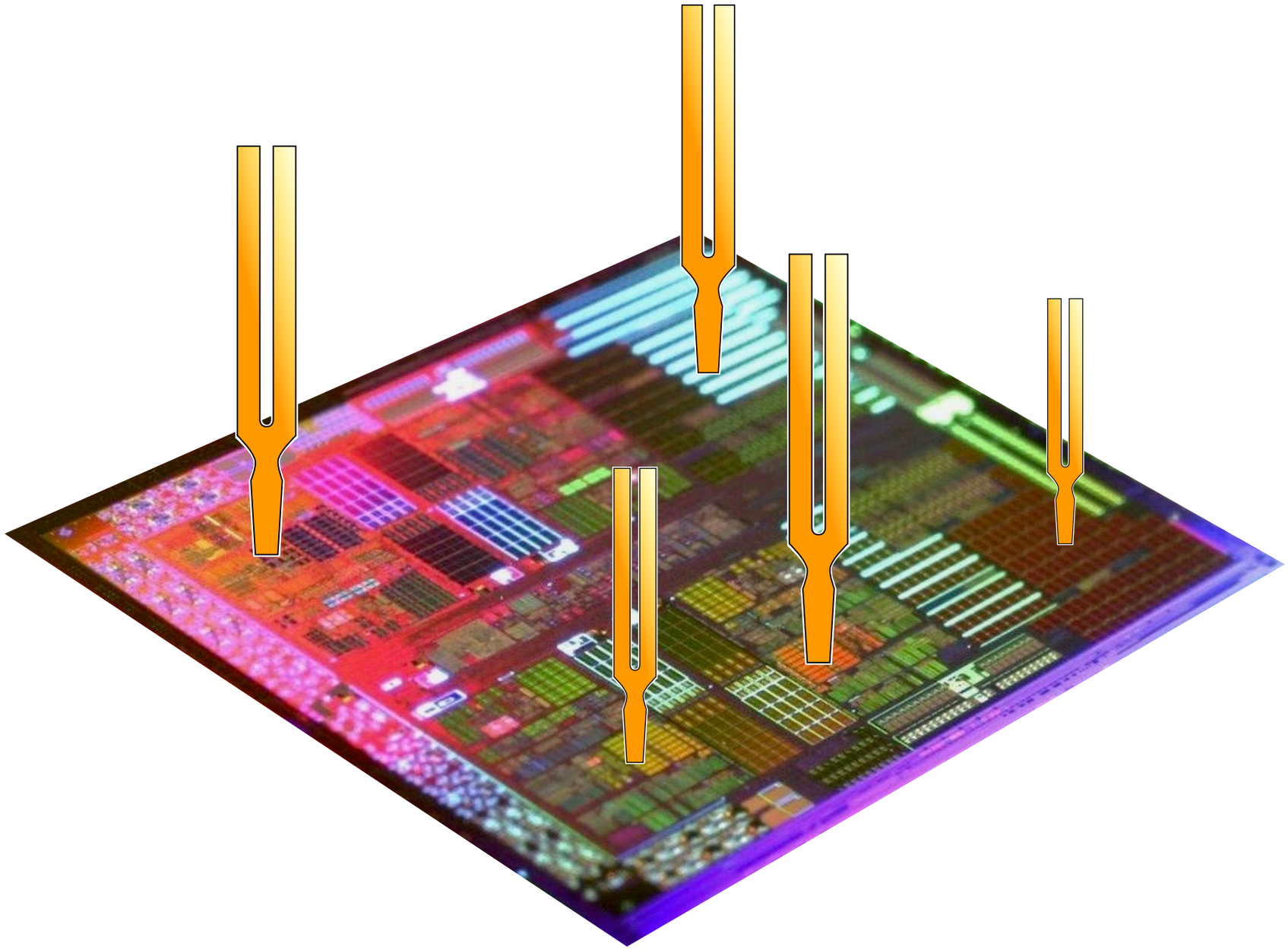
PLLs are so good!

Why are we fussing?

- PLLs are intentionally slow to respond to changes!
- We require the clock frequency to adapt more rapidly to changes.

Future?

Rapid adjustment and tuning of clocks:



Outline

Part 1:

- Overview
- Intro to PLLs
- Clocking with PLLs
- Analog PLLs

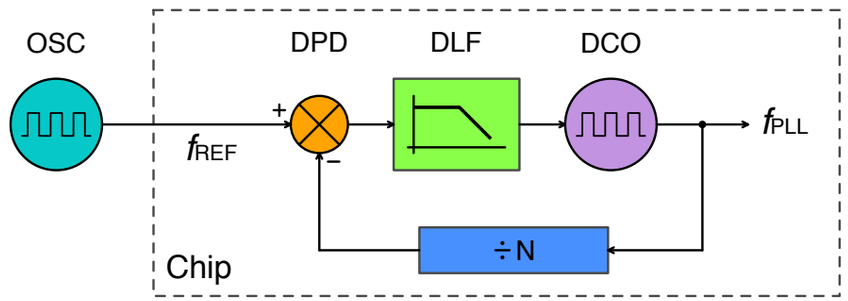
Part 2:

- Recap
- Digital PLLs
- Future challenges
- Summary

Summary

- PLLs are the greatest thing since sliced bread!
- Stable & low jitter = more computing per clock cycle.
- PLLs enable reliable data transfers.
- Large power hungry circuits => move to digital PLLs.
- Future needs:
  – responsive clock generators
  – clock tuning schemes

Discussion Session #2



- What's not clear?
- Why have PLLs become the main way to generate on-chip clocks?
- Why are analog PLLs still the most common?
- Why are digital PLLs becoming popular?
- Other future needs?

Happy Holidays!

See you in 2021!